CORNERSTONE

Quick reference design guidelines for the fifth fabrication call – November 2017

Mask submission deadline – Friday 12th January 2018

File format = *.gdsII*.

Manufacturing grid size = 1 nm.

Design area = **11.47 x 4.9 mm²**, with 0.5 mm bleed regions on the east and west facets if desired.

SOI platform = 340 nm Si / 2 µm BOX.

1. Design rules summary

A summary of the design rules and GDS layer numbers can be found in Table 1 below.

Table 1 – Design rules summary.

Layer description	GDS number	Field	Min. feature size
Silicon Etch 1 (140 nm ± 10 nm)	6	Dark	250 nm
Silicon Etch 2 (240 nm ± 10 nm)	3	Light	250 nm
	4	Dark	
Silicon Etch 3 (100 nm to BOX)	5	Light	250 nm
Cell Outline	99	N/a	N/a
Bleed Area	98	N/a	N/a

2. Minimum feature sizes, tolerances and other design rules

- Minimum feature sizes for each GDS layer are detailed in Table 1.
- A minimum spacing between waveguides of at least 5 µm is recommended to avoid power coupling.
- All structures drawn in GDS layer 6 (Grating couplers) must extend outside of GDS layer 3 (Waveguides) by at least 200 nm to account for alignment error between layers, and feature rounding. An example grating coupler design is available in the 'CORNERSTONE MPW Run 5 GDSII Template' file.
- All structures drawn in GDS layer 5 (Rib protect) should extend 10 µm beyond the edge of GDS layer 3 (Waveguides), with the exception of rib-to-strip transitions.

3. Technical support

For all queries, email cornerstone@soton.ac.uk.