

The CORNERSTONE Project: UK Silicon Photonics Fabrication Capability



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CORNERSTONE- CAPABILITY FOR OPTOELECTRONICS, METAMATERIALS, NANOTECHNOLOGY, AND SENSING

How to show your research has potential for a wider social/economic impact? → Fabricate devices in an INDUSTRIALLY COMPATIBLE way (DUV photolithography)

Overview: CORNERSTONE is a new rapid prototyping fabrication capability that can provide competitive prices for both active and passive silicon photonic devices, via an MPW service.

Aim: To establish silicon photonics fabrication capability that can support photonics research in the UK, and beyond.

What is Offered?

- Three standard SOI photonic platforms:
 - 220 nm Si / 2 μm BOX, 340 nm Si / 2 μm BOX, and 500 nm Si / 3 μm BOX
- Passive devices fabrication runs:
 - waveguides, MUX, DEMUX, filters,...
- Active devices fabrication runs:
 - modulators,...
- Three Si etch depths for each SOI photonic platform:
 - shallow Si etch step (for grating couplers)
 - intermediate Si etch step (for rib waveguides)
 - full Si etch, to the BOX layer (for strip waveguides)
- Four implantation steps for active runs (2 each for *n*-type, and *p*-type):
 - low and high doping levels for both *n*-type (phosphorus) and *p*-type (boron) implantation steps
- Three metal layers in the BEOL:
 - One layer for ohmic Si contacts
 - Two layers for heaters

University of Glasgow

Chip-level processing
Prof Marc Sorel
Dr Graham Sharp



University of Surrey

Ion implantation
Prof Jonathon England
Prof Roger Webb



University of Southampton

Wafer-scale processing
Prof Graham Reed
Prof Goran Mashanovich
Dr David Thomson
Dr Frederic Gardes
Dr Harold Chong
Dr Callum Littlejohns
Dr Ying Tran
Dr Stevan Stankovic
Dr Han Du
Dr Xingzhao Yan



CORNERSTONE Facilities

- DUV Nikon NSR-S204B scanner
- E-beam lithography
- Nanoimprint lithography
- Contact lithography (i-line)
- Wet & dry etch systems
- Furnaces and RTA systems
- PECVD, LPCVD & ALD systems
- Evaporation & RI sputtering systems
- CMP, wafer dicing,...
- Bonding: wafer, wire, flip-chip
- FIB, SEM, ellipsometry,...
- Ion implantation



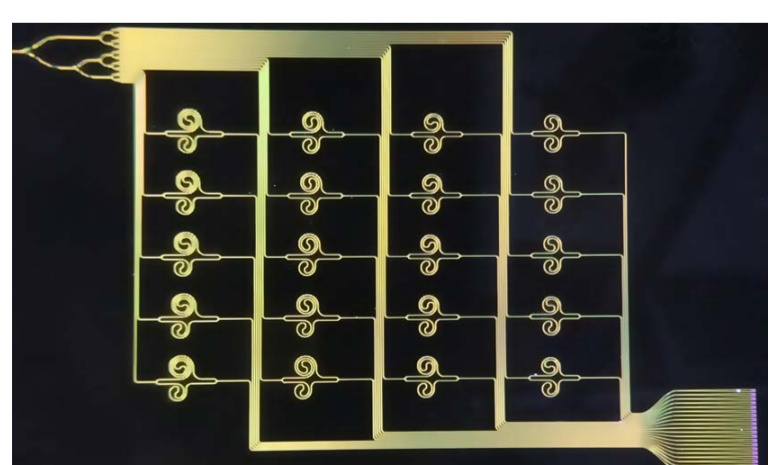
Schedule & Cost

Call	Call Type	Mar. 2018	Apr. 2018	May 21, 2018	Jun. 2018	Jul. 2018	Aug. 2018	Sep. 2018	Oct. 2018	Nov. 2018	Dec. 2018	Jan. 2019	Feb. 2019	Mar. 2019	Apr. 2019	May 2019
		MPW #7 – 340 nm SOI platform	Passive	█	█	█	█	█	█	█	█	█	█	█	█	█
MPW #8 – 220 nm SOI platform	Passive	█	█	█	█	█	█	█	█	█	█	█	█	█	█	█
MPW #9 – 500 nm SOI platform	Passive	█	█	█	█	█	█	█	█	█	█	█	█	█	█	█
MPW #10 – 220 nm SOI platform	Passive	█	█	█	█	█	█	█	█	█	█	█	█	█	█	█
MPW #11 – 220 nm SOI platform	Active	█	█	█	█	█	█	█	█	█	█	█	█	█	█	█
MPW #12 – 340 nm SOI platform	Passive	█	█	█	█	█	█	█	█	█	█	█	█	█	█	█
MPW #13 – 220 nm SOI platform	Passive	█	█	█	█	█	█	█	█	█	█	█	█	█	█	█
MPW #14 – 500 nm SOI platform	Passive	█	█	█	█	█	█	█	█	█	█	█	█	█	█	█

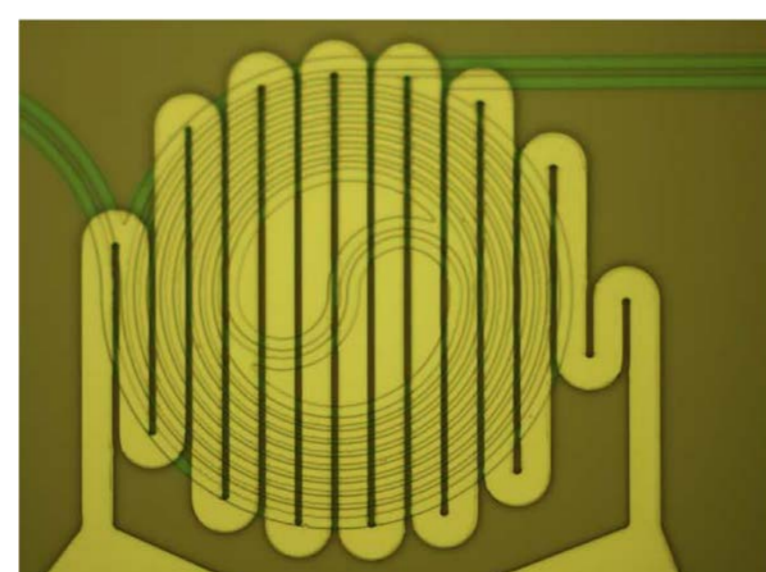
Design area	Active devices	Passives with heaters	Passive devices
11.47 mm x 4.9 mm	£35,000	£10,000	£5,000
5.5 mm x 4.9 mm	£20,000	£7,000	£3,500

Example Capabilities

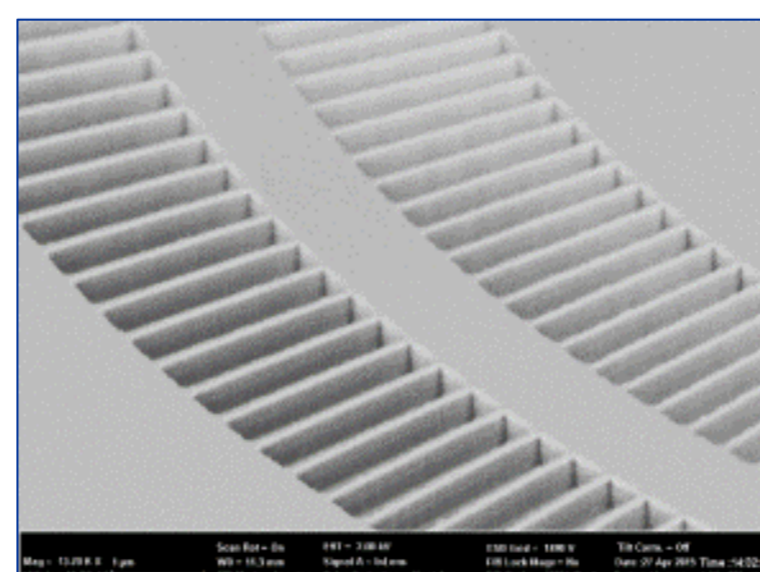
Spectrometers



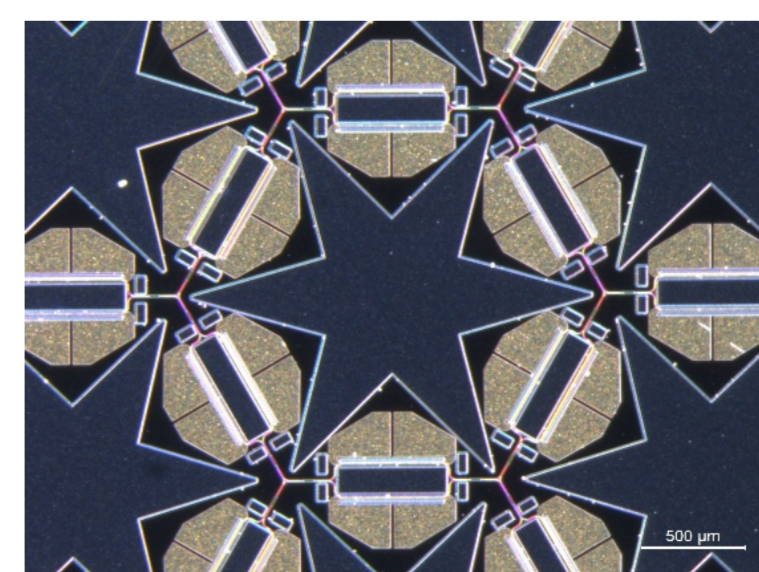
Passives with heaters



Suspended waveguides



Tuneable processor cores



Modulators



Vision: To underpin photonics research in UK and beyond, and support a wide range of research activities