CORNERSTONE

Quick reference design guidelines for the ninth fabrication call – September 2018

Mask submission deadline – Friday 30th November 2018

File format = *.gdsII*.

Manufacturing grid size = 1 nm.

Design area = **11.47 x 4.9 mm²**, with 0.5 mm bleed regions on the east and west facets if desired.

Top cell name: 'Cell0_*[Name of Institution]*'.

1. Changes from previous design rules

The following is a list of major changes from the previous design rules (besides from the SOI platform and etch depths)

1. The minimum feature size for the waveguide layer (GDS layer 3 and GDS layer 4) has been increased to 300 nm. The minimum gap for this layer remains at 250 nm.

2. Design rules summary

A summary of the design rules and GDS layer numbers can be found in Table 1 below.

Table 1 – Design rules summary.

Layer description	GDS number	Field	Min. feature size	Min. gap	Max. feature width
Silicon Etch 1 (160 nm ± 15 nm)	6	Dark	250 nm	250 nm	N/a
Silicon Etch 2 (300 nm ± 20 nm)	3	Light	300 nm	250 nm	N/a
	4	Dark			
Cell Outline	99	N/a	N/a	N/a	N/a
Bleed Area	98	N/a	N/a	N/a	N/a

* Since this call only offers rib waveguides, all features drawn in GDS layer 3 and GDS layer 4 must be covered with GDS layer 5, as in the 'CORNERSTONE MPW Run 9 GDSII Template' file. This is to ensure that designs submitted to this call are compatible with future calls that offer both rib and strip waveguides.

3. Minimum feature sizes, tolerances and other design rules

- Minimum feature sizes and maximum feature widths (where applicable) for each GDS layer are detailed in Table 1.
- A minimum spacing between waveguides of at least 5 µm is recommended to avoid power coupling.
- All structures drawn in GDS layer 6 (Grating couplers) must overlap by at least 200 nm with GDS layer 3 (Waveguides).
- All structures drawn in GDS layer 5 (Rib protect) should extend 10 µm beyond the edge of GDS layer 3 (Waveguides).

4. Technical support

For all queries, email cornerstone@soton.ac.uk.