# CORNERSTONE

## Design guidelines for Ge-on-Si MPW #3 – May 2023

## Sign-up deadline – Friday 30th June 2023

## Mask submission deadline – Friday 28th July 2023

### 1 Terms & conditions and cost

All design submissions must agree with the terms and conditions:

www.cornerstone.sotonfab.co.uk/terms-and-conditions

Under no circumstances will we accept designs without agreement with the terms.

Therefore, we strongly recommend that the terms and conditions are pre-authorised by your institution prior to the mask submission date.

A purchase order (PO) must be uploaded at the same time as submitting your mask design in order pay the access fee, detailed in Table 1 below. Purchase orders will not be accepted via email.

*Table 1 – Access cost.*

| Design Area | Access Cost* |
|---|---|
| 11.47 x 15.45 $mm^2$ | £5,250 |

*Quoted prices are exclusive of VAT, import duties/customs fees, withholding taxes etc.

For information about setting up CORNERSTONE as a supplier to your institution, please contact cornerstone@soton.ac.uk.

Section 7 details the design submission process in more detail.

### 2 Changes from previous Ge-on-Si MPW call

- *.oas* file type added as an acceptable file format for design submissions.

### 3 Process design kit

For the Ge-on-Si platform which is designed to support a wide range of wavelengths in the mid-IR (~2-14 µm), there is not yet a detailed PDK of components because there is no clear choice in wavelength range to choose for the PDK components.

Therefore, the GDSII template file only contains the outline of the cell and the layer descriptions at this time.

### 4 Process flow

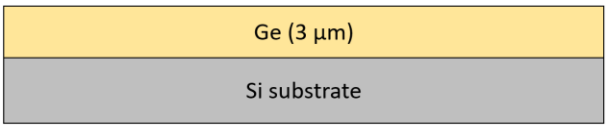
For this call, the patterns will be processed on a single-side polished silicon wafer, with the following nominal parameters:

- Crystalline silicon (Si) substrate
- Crystalline germanium (Ge) core layer (100)-oriented with a thickness $h_{wg}$ = 3 µm ± 200 nm

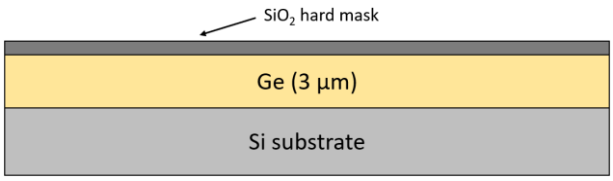
We will offer one germanium etch process: 1) a partial germanium etch of 1.8 µm, followed by a dicing process to form optical facets for edge couplers.

The schematic description of the process flow is given below:

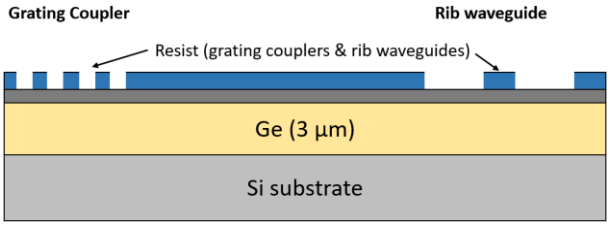
1. Starting Ge-on-Si substrate



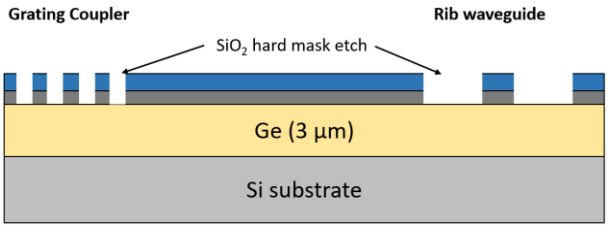

2. Hard mask ($SiO_2$) deposition – 400nm



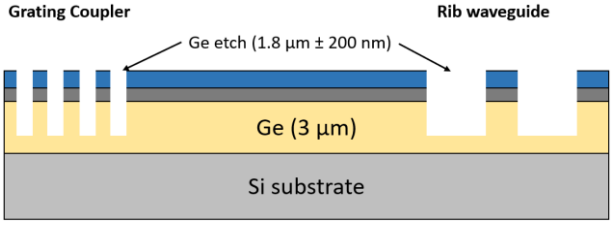

3. Resist patterning for grating couplers and waveguides – GDS layer 304



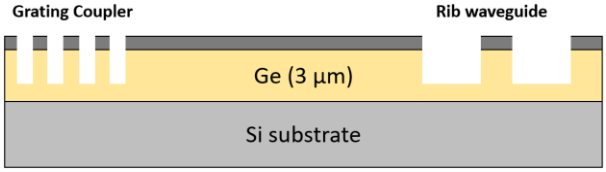

4. Hard mask etch



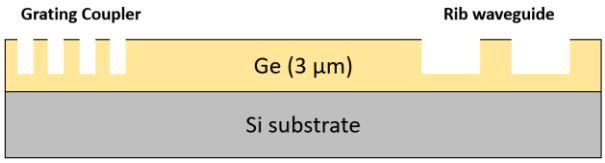

5. Partial Ge etch – 1.8 µm ± 200 nm




6. Resist strip



7. Hard mask HF etch




8. Facet preparation by dicing

If you require any alternative processing steps (e.g. custom etch depths), we may be able to perform them for an additional charge. Email cornerstone@soton.ac.uk with your request.

## 5 Design rules

It is important that designs conform to the following design rules to ensure correct processing.

### 5.1 Design area

The standard user cell has dimensions of **11.47 x 15.45 mm²**, as shown in Figure 1.

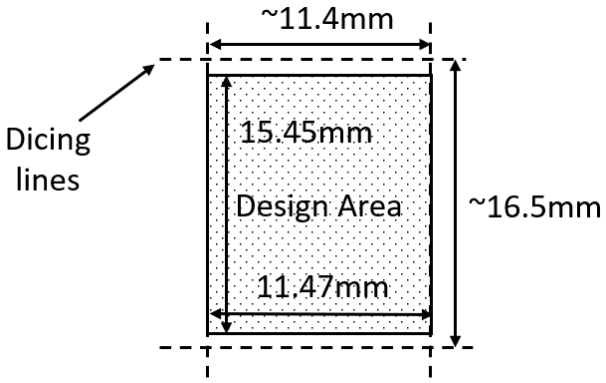



*Figure 1: Dicing process and physical die dimensions after dicing.*

The east and west facets will be diced to produce optical facets for edge coupling. Therefore, if you require edge couplers, ensure that your waveguides extend fully into the bleed region defined as a 35 µm strip at the edge of the east and west edges (see Section 5.2). As this region will be diced, ensure that no other devices extend into this region.

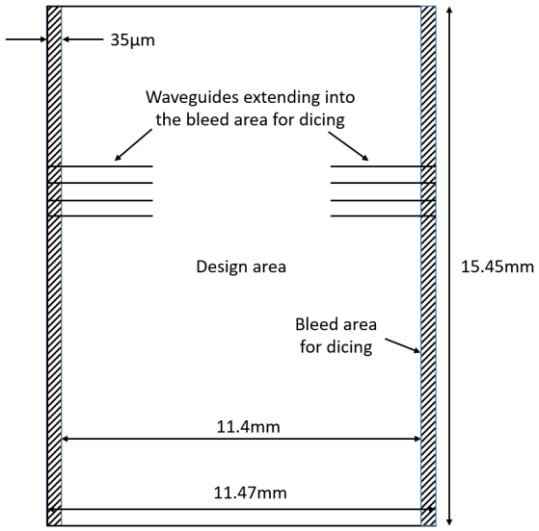



*Figure 2: Bleed area for the dicing process for edge couplers.*

## 5.2 GDS layers

Each lithographic step in the fabrication process flow is identified by a specific GDS layer/s. These are as follows:

*Germanium Etch 1 (Waveguide layer) – GDS Layer 303 (Light field) & GDS Layer 304 (Dark field) – etch depth: 1.8 µm ± 200 nm.*

This layer defines waveguides and is split into two separate GDS layer numbers, patterned into the same resist and etched together:

*GDS Layer 303*: Drawn objects on this layer will be protected from the germanium etch. Users should draw the waveguides and any other features to remain following 1.8 µm germanium etching. During fracturing processing, this will be translated into a pattern that defines 20 µm wide trenches on either side of the waveguides drawn in GDS layer 303 (see Figure 3).

If you require waveguide trenches that are a different width, refer to the guidelines for generating the trenches in Section 8. You can complete these steps yourself and modify the growth function dimension in step 1.

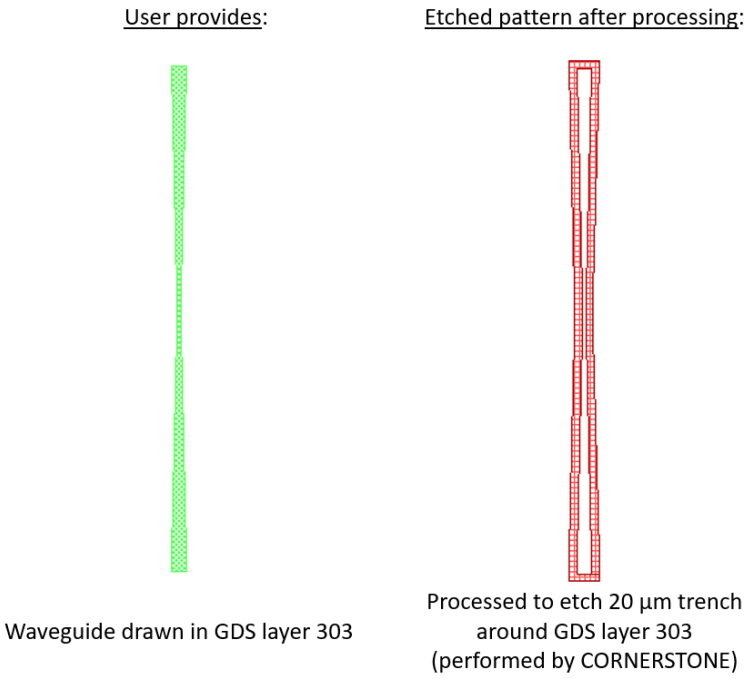



*Figure 3 - Description of GDS Layer 303 processing.*

*GDS Layer 304*: Drawn objects on this layer will be exposed to the 1.8 µm germanium etch. An example photonic crystal structure is shown in Figure 4. The important thing to note here is that the waveguide layer drawn in GDS layer 303 should overlap the structures drawn in GDS layer 304, so that when the 20 µm trenches are generated by CORNERSTONE, a continuous waveguide remains.

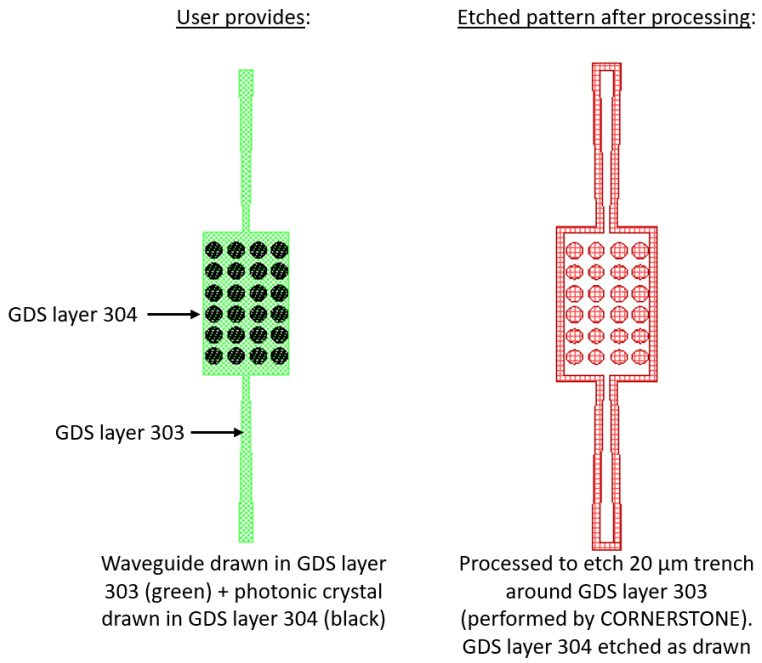



*Figure 4 – Example photonic crystal structure using GDS Layers 303 & 304.*

*Bleed area – GDS Layer 98*

This layer defines the bleed area that will be diced on the east and west facets, as shown in Figure 2.

*Cell Outline – GDS Layer 99*

This layer defines the design space boundaries (11.47 x 15.45 $mm^2$).

*Labels – GDS Layer 100*

This layer defines text labels, which will be merged with Germanium Etch 1 (Waveguides) by the CORNERSTONE team.

*Note:* You do not need to add fabrication alignment marks to your design. Layer-to-layer alignment marks will be added by the CORNERSTONE team, placed outside the design area.

### 5.3 Minimum feature sizes, target critical dimensions and other design rules

- Minimum feature sizes, minimum gaps, and maximum feature widths for each GDS layer are detailed in Table 2.
- The target critical dimension for each GDS layer is listed in Table 2. Note that other feature sizes may have a small dimensional bias.

### 5.4 Design rules summary

A summary of the design rules and GDS layer numbers described in this section is detailed in Table 2 below.

*Table 2 – Design rules summary.*

| Layer description | GDS number | Field | Min. feature size | Min. gap | Target lithography critical dimension |
|---|---|---|---|---|---|
| Germanium Etch 1 (1.8 µm ± 200 nm) | 303 | Light | 700 nm | 700 nm | 700 nm |
| | 304 | Dark | 700 nm | 700 nm | |
| Bleed area | 98 | N/a | N/a | N/a | N/a |
| Cell Outline | 99 | N/a | N/a | N/a | N/a |
| Labels* | 100 | Dark | 700 nm | 700 nm | N/a |

*Features drawn in the Labels layer will be merged into Germanium Etch 1 by the CORNERSTONE team.

If you have access to Tanner L-Edit software, on our website you can find a .tdb version of the template containing a DRC file that you can run to automatically find any design rule violations (note that the automatic DRC will not check all of the design rules, so it remains very important to read the design rules in detail).

### 5.5 File format

Designs must be submitted in a Graphical Database System file format (extension *.gdsII*) ) or Open Artwork System Interchange Standard (extension *.oas*) format. Ensure a manufacturing grid size of 1 nm is used.

We recommend dedicated lithography editing software be used in the design of the *.gdsII* file or *.oas* file.

### 5.6 GDSII template file

A *.gdsII* template file has been made available containing the information described in this section. Ensure that all submitted designs fit within the specified area, and that only the designated GDS layer numbers are used.

## 6 Quality assessment

This fabrication run will be qualified by characterising a standard test pattern that is included on the chip (not part of the user cell). The test structures that will be checked after fabrication are reported in Table 3 below, together with the values that are targeted by the CORNERSTONE platform.

*Table 3 – Quality assessment parameters.*

| Test structure | Parameter | Value |
|---|---|---|
| Straight single mode rib waveguide | Propagation loss | < 5 dB/cm for TE mode at λ = 3.8 µm |

## 7 Mask submission procedure

In order to be eligible to submit a design you must first sign-up to this call using the online form found using the link below. This is in order to enable us to prepare the necessary paperwork and plan the fabrication process effectively. The sign-up deadline is found at the top of this document.

www.cornerstone.sotonfab.co.uk/work-with-us/sign-up-form

Under no circumstances will we accept any design submissions for which we have not received a sign-up form.

After completing the sign-up form, when you are ready to submit your mask design on or before the mask submission deadline listed at the top of this document, follow the link below to the CORNERSTONE website mask submission page:

www.cornerstone.sotonfab.co.uk/work-with-us/mask-submission-form

A purchase order (PO) must be uploaded to this form to pay the access fee. Purchase orders will not be accepted via email.

After completion of the mask submission form, you will be emailed instructions on how to share your design file with the CORNERSTONE team. Ensure that the top cell in your design file is titled 'Cell0_*[Name of Institution]*'.

For information about setting up CORNERSTONE as a supplier to your institution, please contact cornerstone@soton.ac.uk.

## 8 Mask processing performed by CORNERSTONE

Upon receipt of your *.gdsII* file, the CORNERSTONE team will perform the following mask processing steps in order to produce the final mask, based on the descriptions provided in Section 5.2:

*Germanium Etch 1 (Waveguide layer) – GDS Layer 303 (Light field) & GDS Layer 304 (Dark field) – etch depth:* 1.8 µm ± 200 nm*:*

1. Grow Waveguide Etch layer (GDS layer 303) by 20 µm in all directions.
2. Subtract the Waveguide Etch layer (GDS layer 303) from the output of (1) to produce the etch trenches around the drawn waveguides.
3. Merge the output of (2) with the dark field Waveguide Etch layer (GDS layer 304) and the Labels layer (GDS layer 100).

## 9 Technical support

If you have any questions relating to the fabrication process or design rules, please contact the CORNERSTONE team (cornerstone@soton.ac.uk).

## 10 Device delivery

A total of 5 replica cells will be delivered to each user. A tentative delivery date of October 2023 has been set.

## 11 Feedback

Feedback is essential to the CORNERSTONE team. It is required to ensure a continuous improvement to the quality of our services. It is also evidence on the user satisfaction, and a measure to what extent we were able to meet user requirements. Therefore, we kindly ask our users to provide feedback to us, including device performance data, SEM images, future interests for the CORNERSTONE project etc. A feedback form will be sent to you along with your chips.

Alternatively, email cornerstone@soton.ac.uk with your comments.

## 12 Publication

Please include CORNERSTONE in the acknowledgments section of any publications that result from the chips you receive from CORNERSTONE.