CORNERSTONE

Design guidelines for SiN MPW 7 – October 2023

Sign-up deadline – Friday 1st December 2023

Revised mask submission deadline – Wednesday 3rd January 2024

1 Terms & conditions and cost

All design submissions must agree with the terms and conditions:

www.cornerstone.sotonfab.co.uk/terms-and-conditions

Under no circumstances will we accept designs without agreement with the terms.

Therefore, we strongly recommend that the terms and conditions are pre-authorised by your institution prior to the mask submission date.

A purchase order (PO) must be uploaded at the same time as submitting your mask design in order pay the access fee, detailed in Table 1 below. Purchase orders will not be accepted via email.

Table 1 – Access cost.

Design Area	Access Cost with heaters*	Access Cost without heaters*
11.47 x 15.45 mm^2	£11,900	£5,800

*Quoted prices are exclusive of VAT, import duties/customs fees, withholding taxes etc.

For information about setting up CORNERSTONE as a supplier to your institution, please contact cornerstone@soton.ac.uk.

Section 8 details the design submission process in more detail.

1.1 Discounted access

We are launching a new initiative to encourage our users to include the Engineering and Physical Sciences Research Council (EPSRC) funded CORNERSTONE (EP/L021129/1) or CORNERSTONE 2 (EP/T019697/1) projects in the "*Funding*" section of relevant journal publications. This is important to us to be able to demonstrate impact from the funding.

Therefore, if you are able to share the digital object identifier (DOI), we will give you a 5% discount from the access charges listed in Table 1 above for your first published journal paper and 10% for two and more journal papers that reference one of the CORNERSTONE projects.

2 Design rule changes from previous call (SiN MPW #6)

- No change

3 IPKISS process design kit

For the greatest functionality, we recommend that you use Luceda's IPKISS software to access the process design kit (PDK), after purchasing the required license. The IPKISS platform enables the automation and integration of all aspects of your photonic design flow in one tool, using one standard

language. The PDK can be used in either IPKISS' Python coding environment or in the GUI of Siemens EDA L-Edit by using the IPKISS Link for Siemens EDA.

To obtain a copy of the software and a license key, please contact Luceda by sending an email to info@lucedaphotonics.com, specifying that you require a license for CORNERSTONE PDK usage. Luceda will contact you within 1-2 working days following the receipt of your request to provide a quote for the license. Of course, if you already have a valid license, the PDK can be accessed free of charge.

For more information about Luceda's software offering, please visit www.lucedaphotonics.com.

Once you have access to the Luceda software, to obtain a copy of the CORNERSTONE PDK, please contact Luceda support at info@lucedaphotonics.com. An account will be created for you at support.lucedaphotonics.com for any technical support on Luceda's IPKISS software or the CORNERSTONE PDK implementation.

We also have a PDK available for download in *.gdsII* format.

4 Process flow

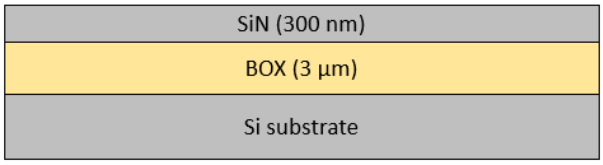
For this call, the patterns will be processed on a single-side polished SiN-on-Insulator (SiNOI) wafer, with the following nominal parameters:

- Crystalline silicon (Si) substrate
- Thermal silica (SiO_2) Buried OXide (BOX) layer with a thickness h_{box} = 3 µm
- LPCVD Silicon nitride (SiN) core layer h_{wg} = 300 nm ± 15 nm

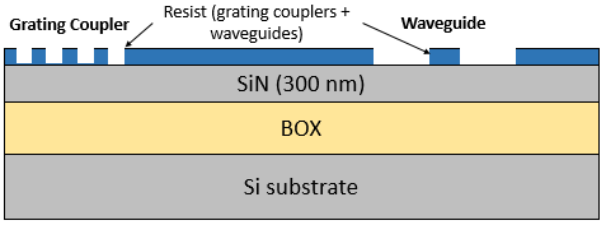
We will offer one silicon nitride etch process: 1) a full silicon nitride etch to the BOX layer. We will offer a 2 µm ± 200 nm thick silicon dioxide top cladding layer with two metal layers for heaters: 1) heater filaments, and 2) heater contact pads.

The schematic description of the process flow is given below:

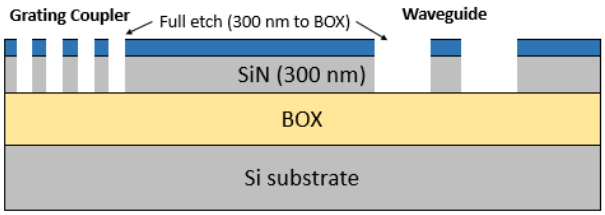
1. Starting SiNOI substrate



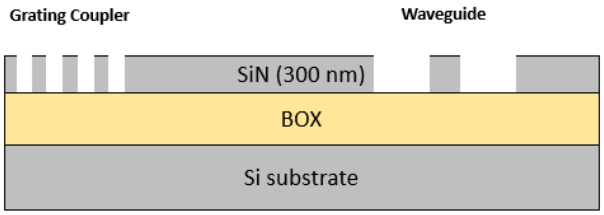
2. Resist patterning for SiN Etch (GDS layers 203 & 204) – 300 nm etch to BOX



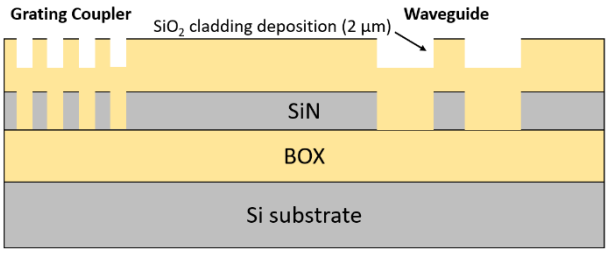
3. SiN etch (300 nm etch to BOX)



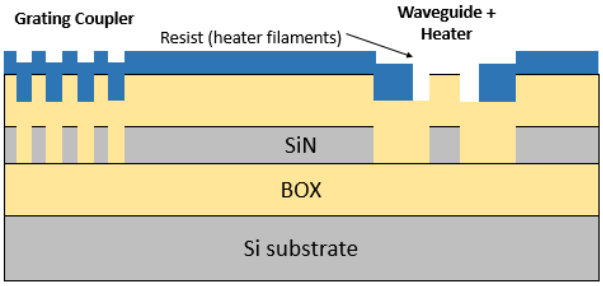
4. Resist strip



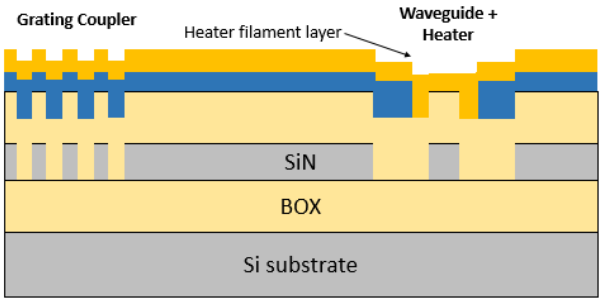
5. Silicon dioxide cladding deposition – 2 µm



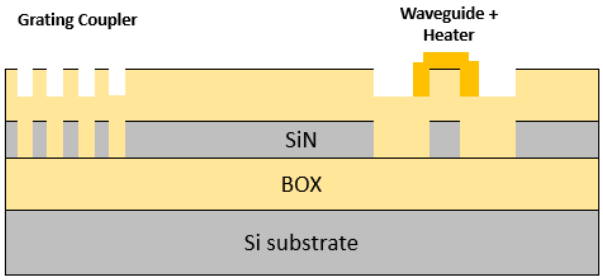
6. Resist patterning for Heater Filaments (GDS layer 39)



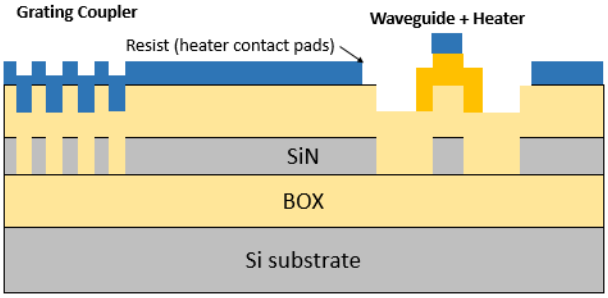
7. Heater filament deposition



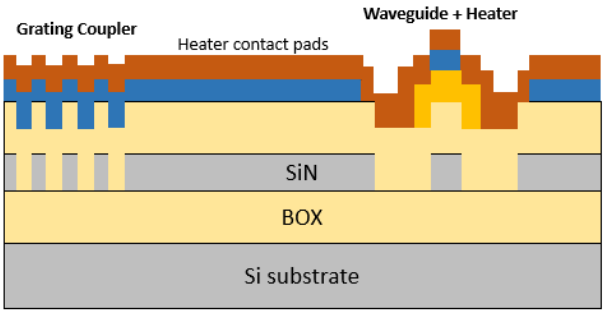
8. Metal lift-off



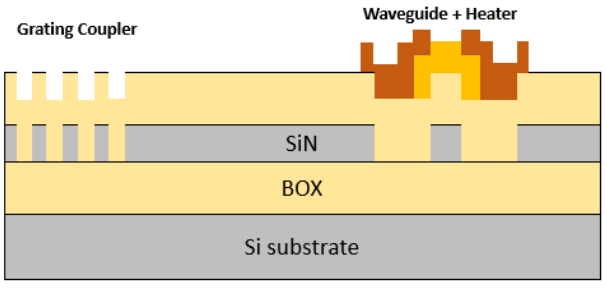
9. Resist patterning for Heater Contact Pads (GDS layer 41)



10. Heater contact pads deposition



11. Metal lift-off



If you require any alternative processing steps (e.g. additional etch depths, selective cladding openings), we may be able to perform them for a small charge. Email cornerstone@soton.ac.uk with your request.

5 Design rules

It is important that designs conform to the following design rules to ensure clarity and correct processing.

5.1 Design area

The standard user cell has dimensions of **11.47 x 15.45 mm^2**.

5.1.1 Physical die size

The physical size of the dies you will receive is approximately 12.5 x 16.5 mm^2. This area includes a border the CORNERSTONE team will add that contains alignment marks, metrology boxes etc.

5.2 GDS layers

Each lithographic step in the fabrication process flow is identified by a specific GDS layer/s. These are as follows:

Silicon Nitride Etch 1: 300 nm full etch to BOX – GDS Layer 203 (Light field): Drawn objects on this layer will be protected from the silicon nitride etch. Users should draw the waveguides and any other features to remain following the full silicon nitride etching. During fracturing processing, this will be translated into a pattern that defines 5 µm wide trenches on either side of the waveguides drawn in GDS layer 203 (see Figure 1).

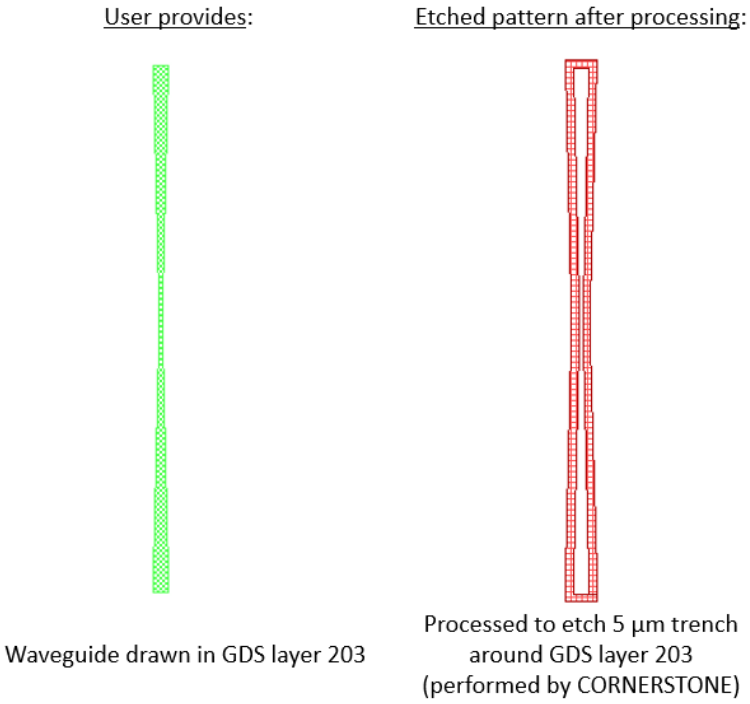


Figure 1 - Description of GDS Layer 203 processing.

If you require waveguide trenches that are a different width, refer to the guidelines for generating the trenches in Section 9. You can complete these steps yourself and modify the growth function dimension in step 1.

- *Silicon Nitride Etch 1: 300 nm full etch to BOX – GDS Layer 204 (Dark field)*: Drawn objects on this layer will be exposed to the silicon nitride full etch to the BOX. An example photonic crystal structure is shown in Figure 2. The important thing to note here is that the waveguide layer drawn in GDS layer 203 should overlap the structures drawn in GDS layer 204, so that when the 5 µm trenches are generated by CORNERSTONE, a continuous waveguide remains. Note that the client should contact CORNERSTONE team if the design has photonic crystals structures with a diameter smaller than 600 nm to decide on whether structures need to be biased.

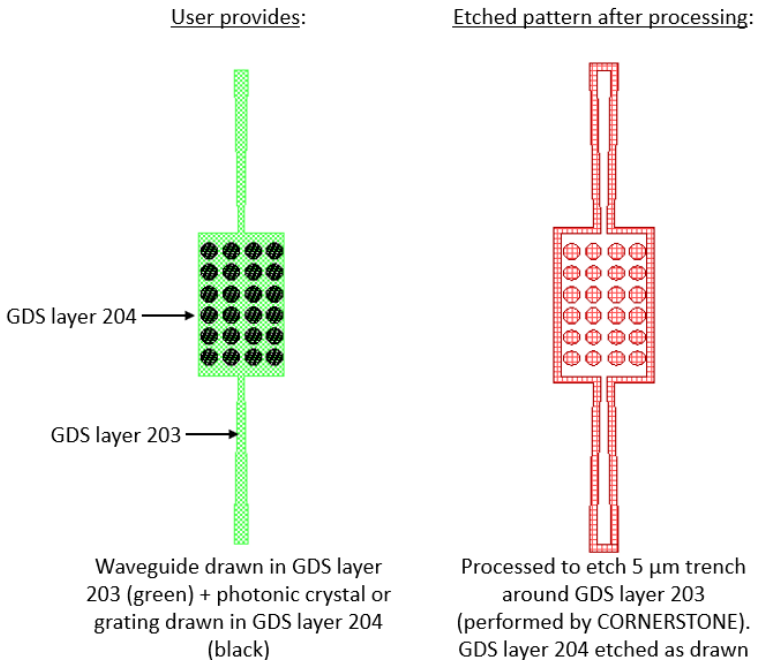


Figure 2 – Example photonic crystal structure using GDS Layers 203 & 204.

Heater Filaments – GDS Layer 39 (Light field)

This layer defines the heater filaments. Drawn objects on this layer will remain after metal lift-off. It is recommended to use a filament width of 900 nm for the best compromise between heater power efficiency, phase tunability and robustness.

Heater Contact Pads – GDS Layer 41 (Light field)

This layer defines the heater contact pads. Drawn objects on this layer will remain after metal lift-off.

An example heater layout for a straight waveguide is included in the *.gdsII* template file. The contact pads can be modified according to your probe design.

Cell Outline – GDS Layer 99

This layer defines the design space boundaries.

Labels – GDS Layer 100

This layer defines text labels, which will be merged with Silicon Nitride Etch 1 layer by the CORNERSTONE team. This layer will not have any design rule checking (DRC) performed.

Note: You do not need to add fabrication alignment marks to your design. Layer-to-layer alignment marks will be added by the CORNERSTONE team, placed outside the design area.

5.3 Minimum feature sizes, target critical dimensions and other design rules

- Minimum feature sizes, minimum gaps, and maximum feature widths for each GDS layer are detailed in Table 2.
- The target critical dimension for each GDS layer is listed in Table 2. Note that other feature sizes may have a small dimensional bias.
- A minimum spacing between waveguides of at least 10 µm is recommended to avoid power coupling.
- An overlap of at least 2 µm between GDS layer 39 (Heater Filaments) and GDS layer 41 (Heater Contact Pads) is recommended for optimal heater performance.
- The client should contact CORNERSTONE team if GDS Layer 204 has photonic crystals structures with a diameter smaller than 600 nm to decide on whether structures need to be biased.

5.4 Design rules summary

A summary of the design rules and GDS layer numbers described in this section is detailed in Table 2 below.

Table 2 – Design rules summary

Layer description	GDS number	Field	Min. feature size	Min. gap	Max. feature length	Target lithography critical dimension
Silicon Nitride Etch 1 (300 nm full etch to BOX)*	203	Light	250 nm	250 nm	20 µm	660 nm
			350 nm	250 nm	N/a	
	204	Dark	250 nm	250 nm	20 µm	
			250 nm	350 nm	N/a	
Heater Filaments	39	Light	600 nm	10 µm	N/a	900 nm
Heater Contact Pads	41	Light	2 µm	10 µm	N/a	2 µm
Cell Outline	99	N/a	N/a	N/a	N/a	N/a
Labels†	100	Dark	250 nm	250 nm	N/a	N/a

*For the waveguide layer there is a maximum feature length restriction of 20 µm when the minimum feature is 250 nm. This is because resist features that are long and thin can collapse during the development process. Resist widths of > 350 nm are stable and therefore there are no length restrictions for widths > 350 nm.

†Features drawn in the Labels layer will be merged into the Silicon Nitride Etch 1 layer by the CORNERSTONE team.

In order to help you ensure that you comply with the design rules, you can also download a design rule check (DRC) checklist from our website and if you have access to Tanner L-Edit software, a .tdb version of the template containing a DRC file that you can run to automatically find any design rule violations (note that the automatic DRC will not check all of the design rules, so it remains very important to read the design rules in detail). In addition, you can run the KLayout pre-DRC script provided by CORNERSTONE (Please check the user guide to perform the script in KLayout).

5.5 File format

Designs must be submitted in a Graphical Database System file (extension *.gdsII*) or Open Artwork System Interchange Standard (extension *.oas*) format. Ensure a manufacturing grid size of 1 nm is used, as per the CORNERSTONE GDSII Template file.

We recommend dedicated lithography editing software be used in the design of the *.gdsII* or *.oas* file.

5.6 GDSII template file

A *.gdsII* template file has been made available on our website containing the information described in this section. Ensure that all submitted designs fit within the specified area, and that only the designated GDS layer numbers are used.

6 Material properties

The measured refractive index of the LPCVD silicon nitride layer is shown in Figure 3 below. This data is also available in tabular format on our website.

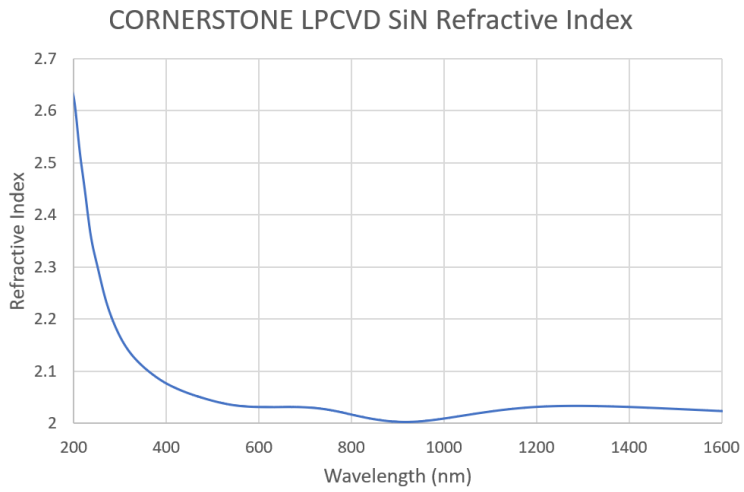


Figure 3 – Silicon nitride refractive index.

7 Quality assessment

This fabrication run will be qualified by characterising a standard test pattern that is included on the chip (not part of the user cell). The test structures that will be checked after fabrication are reported in Table 3 below, together with the values that are targeted by the CORNERSTONE platform.

Table 3 – Quality assessment parameters.

Test structure	Parameter	Value
Straight single mode strip waveguide	Propagation loss	< 0.6 dB/cm for TE mode in C-band

8 Mask submission procedure

In order to be eligible to submit a design you must first sign-up to this call using the online form found using the link below. This is in order to enable us to prepare the necessary paperwork and plan the fabrication process effectively. The sign-up deadline is found at the top of this document.

https://www.cornerstone.sotonfab.co.uk/how-to-access-cornerstone/#mpwform

Under no circumstances will we accept any design submissions for which we have not received a sign-up form.

After completing the sign-up form, when you are ready to submit your mask design on or before the mask submission deadline listed at the top of this document, follow the link below to the CORNERSTONE website mask submission page:

https://www.cornerstone.sotonfab.co.uk/gds-file-upload

A purchase order (PO) must be uploaded to this form to pay the access fee. Purchase orders will not be accepted via email.

After completion of the mask submission form, you will be emailed instructions on how to share your design file with the CORNERSTONE team. Ensure that the top cell in your design file is titled 'Cell0_*[Name of Institution]*'.

For information about setting up CORNERSTONE as a supplier to your institution, please contact cornerstone@soton.ac.uk.

9 Mask processing performed by CORNERSTONE

Upon receipt of your *.gdsII* file, the CORNERSTONE team will perform the following mask processing steps in order to produce the final mask, based on the descriptions provided in Section 5.2:

Silicon Nitride Etch 1 GDS 203 (Light Field) – waveguides & GDS Layer 204 (Dark field) – gratings:

1. Grow Waveguide layer (GDS layer 203) by 5 µm in all directions.
2. Subtract the Waveguide layer (GDS layer 203) from the output of (1) to produce the etch trenches around the drawn waveguides.
3. Merge the output of (2) with the dark field Silicon Nitride Etch layer (GDS layer 204) and the Labels layer (GDS layer 100).

10 Technical support

If you have any questions relating to the fabrication process or design rules, please contact the CORNERSTONE team (cornerstone@soton.ac.uk).

11 Device delivery

A total of 10 replica cells will be delivered to each user. A tentative delivery date of March 2024 has been set.

12 Feedback

Feedback is essential to the CORNERSTONE team. It is required to ensure a continuous improvement to the quality of our services. It is also evidence on the user satisfaction, and a measure to what extent

we were able to meet user requirements. Therefore, we kindly ask our users to provide feedback to us, including device performance data, SEM images, future interests for the CORNERSTONE project etc. A feedback form will be sent to you along with your chips.

Alternatively, email cornerstone@soton.ac.uk with your comments.

13 Publications

Please include CORNERSTONE in the acknowledgments section of any publications that result from the chips you receive from CORNERSTONE.