CORNERSTONE

Quick reference design guidelines for SiN MPW 7 – October 2023

Sign-up deadline – Friday 1st December 2023

Revised mask submission deadline – Wednesday 3rd January 2024

File format = *.gdsII or .oas*

Manufacturing grid size = 1 nm.

Design area = **11.47 x 15.45 mm^2**.

Top cell name: 'Cell0*_[Name of Institution]*'.

1. Terms & conditions and cost

All design submissions must agree with the terms and conditions:

www.cornerstone.sotonfab.co.uk/terms-and-conditions

Under no circumstances will we accept designs without agreement with the terms.

Therefore, we strongly recommend that the terms and conditions are pre-authorised by your institution prior to the mask submission date.

A purchase order (PO) must be uploaded at the same time as submitting your mask design in order pay the access fee, detailed in Table 1 below. Purchase orders will not be accepted via email.

Table 1 – Access cost.

Design Area	Access Cost with heaters*	Access Cost without heaters*
11.47 x 15.45 mm^2	£11,900	£5,800

*Quoted prices are exclusive of VAT, import duties/customs fees, withholding taxes etc.

For information about setting up CORNERSTONE as a supplier to your institution, please contact cornerstone@soton.ac.uk.

Section 8 of the full design rules details the design submission process in more detail.

2. Design rules summary

A summary of the design rules and GDS layer numbers can be found in Table 2 below.

Table 2 – Design rules summary

Layer description	GDS number	Field	Min. feature size	Min. gap	Max. feature length	Target critical dimension
Silicon Nitride Etch 1 (300 nm full etch to BOX)*	203	Light	250 nm	250 nm	20 µm	660 nm
			350 nm	250 nm	N/a	
	204	Dark	250 nm	250 nm	20 µm	
			250 nm	350 nm	N/a	
Heater Filaments	39	Light	600 nm	10 µm	N/a	900 nm
Heater Contact Pads	41	Light	2 µm	10 µm	N/a	2 µm
Cell Outline	99	N/a	N/a	N/a	N/a	N/a
Labels†	100	Dark	250 nm	250 nm	N/a	N/a

*For the waveguide layer there is a maximum feature length restriction of 20 µm when the minimum feature is 250 nm. This is because resist features that are long and thin can collapse during the development process. Resist widths of > 350 nm are stable and therefore there are no length restrictions for widths > 350 nm.

†Features drawn in the Labels layer will be merged into the Silicon Nitride Etch 1 layer by the CORNERSTONE team.

In order to help you ensure that you comply with the design rules, you can also download a design rule check (DRC) checklist from our website and if you have access to Tanner L-Edit software, a .tdb version of the template containing a DRC file that you can run to automatically find any design rule violations (note that the automatic DRC will not check all of the design rules, so it remains very important to read the design rules in detail). In addition, you can run the KLayout pre-DRC script provided by CORNERSTONE (Please check the user guide to perform the script in KLayout).

3. Minimum feature sizes, tolerances and other design rules

- Minimum feature sizes, minimum gaps, and maximum feature widths for each GDS layer are detailed in Table 2.
- The target critical dimension for each GDS layer is listed in Table 2. Note that other feature sizes may have a small dimensional bias.
- A minimum spacing between waveguides of at least 10 µm is recommended to avoid power coupling.
- An overlap of at least 2 µm between GDS layer 39 (Heater Filaments) and GDS layer 41 (Heater Contact Pads) is recommended for optimal heater performance.
- The client should contact CORNERSTONE team if GDS Layer 204 has photonic crystals structures with a diameter smaller than 600 nm to decide on whether structures need to be biased.

4. Technical support

For all queries, email cornerstone@soton.ac.uk.