CORNERSTONE

Quick reference design guidelines for 340 nm SOI Passive MPW #36 – January 2024

Sign-up deadline – Friday 1st March 2024

Mask submission deadline – Wednesday 27th March 2024

File format = *.gdsII or .oas.*

Manufacturing grid size = 1 nm.

Design area = **11.47 x 4.9 mm^2** or **5.5 x 4.9 mm^2**.

Top cell name: 'Cell0_*[Name of Institution]*'.

1.   Terms & conditions and cost

All design submissions must agree with the terms and conditions:

www.cornerstone.sotonfab.co.uk/terms-and-conditions

Under no circumstances will we accept designs without agreement with the terms.

Therefore, we strongly recommend that the terms and conditions are pre-authorised by your institution prior to the mask submission date.

A purchase order (PO) must be uploaded at the same time as submitting your mask design in order pay the access fee, detailed in Table 1 below. Purchase orders will not be accepted via email.

Table 1 – Access cost and Delivery Time.

Design Area	Access Cost with Heaters* (Standard)	Access Cost without Heaters* (Standard)	Access Cost with Heaters* (Priority)	Access Cost without Heaters* (Priority)
11.47 x 4.9 mm^2	£14,250	£9,000	£17,900	£11,300
5.5 x 4.9 mm^2	£10,500	£6,250	£13,200	£7,900
Delivery Time**	14 weeks	14 weeks	7 weeks	5 weeks

*Quoted prices are exclusive of VAT, import duties, withholding taxes etc.

**The indicated delivery time is subject to possible delays that may occur due to scheduled cleanroom maintenance or unforeseen shutdown periods. Users will receive timely notifications regarding any such occurrences.

For information about setting up CORNERSTONE as a supplier to your institution, please contact cornerstone@soton.ac.uk.

Section 7 of the CORNERSTONE 36th Call - Design Rules.pdf document details the design submission process in detail.

2. Discounted access

We encourage our users to include the Engineering and Physical Sciences Research Council (EPSRC) funded CORNERSTONE 2 (EP/T019697/1) or CORNERSTONE 2.5 (EP/W035995/1) projects in the "*Funding*" section of relevant journal publications. This is important to us to be able to demonstrate impact from the funding.

Therefore, if you are able to share the digital object identifier (DOI), we will give you a 5% discount from the access charges listed in Table 1 above for your first published journal paper and 10% for two and more journal papers that reference one of the CORNERSTONE projects.

3. Design rule changes from previous 340 nm SOI platform call (MPW #32)

- *No change*

4. Design rules summary
A summary of the design rules and GDS layer numbers can be found in Table 2 below.

Table 2 – Design rules summary.

Layer description	GDS number	Field	Min. feature size	Min. gap	Max. feature size	Target critical dimension
Silicon Etch 1 (140 nm ± 10 nm)	6	Dark	200 nm	250 nm	20 µm	265 nm
			200 nm	350 nm	N/a	
Silicon Etch 2 (340 nm to BOX)	3	Light	350 nm	200 nm	N/a	450 nm
	4	Dark	200 nm	350 nm		
Heater Filaments	39	Light	600 nm	10 µm	N/a	900 nm
Heater Contact Pads	41	Light	2 µm	10 µm	N/a	2 µm
Cell Outline	99	N/a	N/a	N/a	N/a	N/a
Labels*	100	Dark	250 nm	250 nm	N/a	N/a

*Features drawn in the Labels layer will be merged into Silicon Etch 2 by the CORNERSTONE team.

In order to help you ensure that you comply with the design rules, you can also download a design rule check (DRC) checklist from our website and if you have access to Tanner L-Edit software, a .tdb version of the template containing a DRC file that you can run to automatically find any design rule violations (note that the automatic DRC will not check all of the design rules, so it remains very important to read the design rules in detail).

5. Minimum feature sizes, tolerances and other design rules
- Minimum feature sizes, minimum gaps, and maximum feature widths for each GDS layer are detailed in Table 2.
- The target critical dimension for each GDS layer is listed in Table 2. Note that other feature sizes may have a small dimensional bias.
- A minimum spacing between waveguides of at least 5 µm is recommended to avoid power coupling.
- An overlap of at least 200 nm between GDS layers is essential to account for the alignment tolerance between layers.

- All structures drawn in GDS layer 6 (Grating couplers) must overlap by at least 200 nm with GDS layer 3 (Waveguides).
- An overlap of at least 10 μm between GDS layer 39 (Heater Filaments) and GDS layer 41 (Heater Contact Pads) is recommended for optimal heater performance.
- Ensure all structures drawn in GDS layer 6 (Grating couplers) do not overlap with either GDS layer 39 (Heater Filaments) or GDS 41 (Heater Contact Pads).

6. Technical support

For all queries, email cornerstone@soton.ac.uk.