CORNERSTONE DESIGN GUIDELINES
Ge-on-Si MPW #6 July 2025

SIGN-UP DEADLINE: 13/08/2025
MASK SUBMISSION DEADLINES: 10/09/2025 (SOFT) AND 24/09/2025 (HARD)
All deadlines end at 13:00 (UK time)

1 TERMS & CONDITIONS AND COST

All design submissions must agree with the terms and conditions:

www.cornerstone.sotonfab.co.uk/terms-and-conditions

Under no circumstances will we accept designs without agreement with the terms.

Therefore, we strongly recommend that the terms and conditions are pre-authorised by your institution prior to the mask submission date.

A purchase order (PO) must be uploaded at the same time as submitting your mask design in order pay the access fee, detailed in *Table 1* below. Purchase orders will not be accepted via email.

Table 1 – Access cost and delivery time.

Design Area [mm²]	15.45 x 11.47	Delivery Time
Access Cost (Standard)*	£11,000	10 weeks
Access cost for Enterprises and Academia based in UK†	50% off	As above

*Quoted prices are exclusive of VAT, import duties/customs fees, withholding taxes etc.

†Are you from a UK company or academic institution?

UK companies and universities may be eligible for a 50% discount on the cost of this MPW run with support from the CORNERSTONE Photonics Innovation Centre (C-PIC) (EP/Z531066/1), funded by UK Research and Innovation. Support will be provided under the Subsidy Control Act (2022) via Minimal Financial Assistance. To be eligible you will need to demonstrate the potential impact of receiving assistance against one or more of the following categories: impact on jobs and skills, access to new technology, accelerating product development. Following submission of your sign-up form, you will receive correspondence with more details of how this support will be provided. For UK companies, the support is only available for first time MPW users with a UK design/development/manufacturing presence and only for prototyping and product development.

To receive Design Rule Check (DRC) feedback from the CORNERSTONE team, users must submit their designs no later than the soft deadline. Submissions received after the soft deadline will not be checked against design rules; therefore, any fabrication failures related to design rule violations will be at the users' own risk. The CORNERSTONE team would be grateful for the opportunity to work with you prior to the submission deadline to ensure your designs pass DRC. For more information, please visit our website: www.cornerstone.sotonfab.co.uk/design-rules

For information about setting up CORNERSTONE as a supplier to your institution, please contact cornerstone@soton.ac.uk.

2. DESIGN RULE CHANGES FROM PREVIOUS CALL (MPW #5)

- Standard waveguide and 90-degree bend added to Component Library.

3. PROCESS DESIGN KIT

CORNERSTONE Process Desing Kits (PDK) are available in Luceda Photonics' IPKISS software, GDSFactory, Cadence Virtuoso and L-Edit. PDKs for all CORNERSTONE technology platforms are freely accessible via Wave Photonics' portal. To obtain free access to the PDKs in your preferred software tool, please visit www.wavephotonics.com.

Wave Photonics also provides Scattering Parameters to enable full circuit simulation. For more information, please contact Wave Photonics support at info@wavephotonics.com.

To obtain a copy of the software and a license key for IPKISS, please contact Luceda by sending an email to info@lucedaphotonics.com, specifying that you require a license for CORNERSTONE PDK usage. Luceda will contact you within 1-2 working days following the receipt of your request to provide a quote for the license. Of course, if you already have a valid license, the PDK can be accessed free of charge. The IPKISS platform enables the automation and integration of all aspects of your photonic design flow in one tool, using one standard language. The PDK can be used in either IPKISS' Python coding environment or in the GUI of Siemens EDA L-Edit by using the IPKISS Link for Siemens EDA. For more information, please visit www.lucedaphotonics.com.

A library of building blocks is also available for download in .gdsII format on the CORNERSTONE website: https://www.cornerstone.sotonfab.co.uk/design-rules/

4. PROCESS FLOW

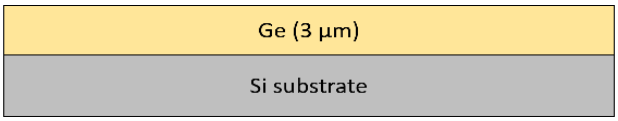
For this call, the patterns will be processed on a single-side polished silicon wafer, with the following nominal parameters:

- Crystalline silicon (Si) substrate
- Crystalline germanium (Ge) core layer (100)-oriented with a thickness h_{wg} = 3 µm ± 200 nm

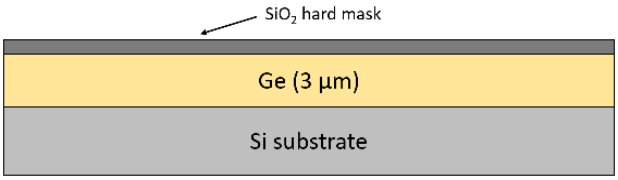
We will offer one germanium etch process: 1) a partial germanium etch of 1.8 µm, followed by a dicing process to form optical facets for edge couplers.

The schematic description of the process flow is given below:

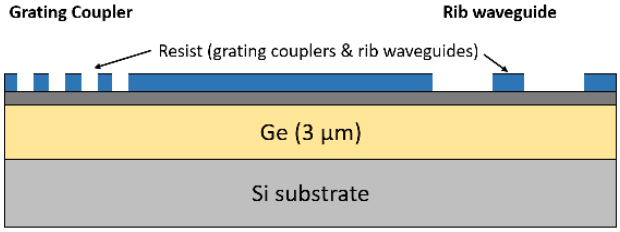
1. Starting Ge-on-Si substrate



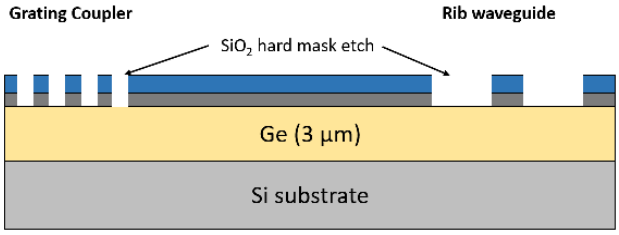
2. Hard mask (SiO_2) deposition – 400nm



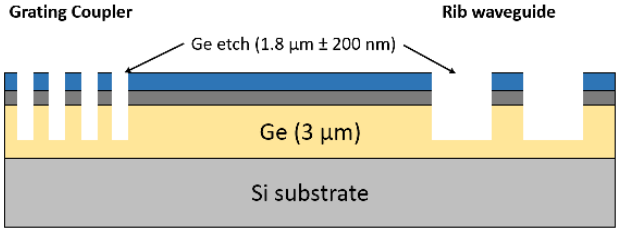
3. Resist patterning for grating couplers and waveguides – GDS layer 303 & 304



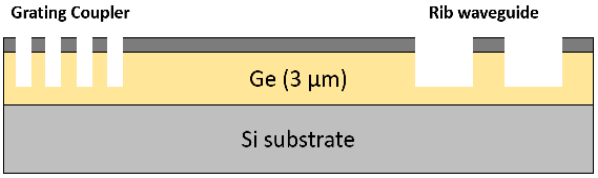
4. Hard mask etch



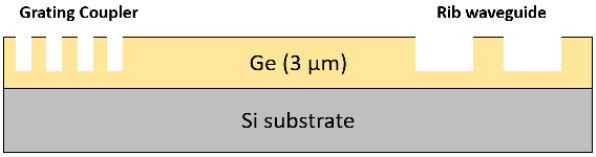
5. Partial Ge etch – 1.8 µm ± 200 nm



6. Resist strip



7. Hard mask HF etch



8. Facet preparation by dicing

If you require any alternative processing steps (e.g. custom etch depths), we may be able to perform them for a suitable charge. Email cornerstone@soton.ac.uk with your request.

5. DESIGN RULES

It is important that designs conform to the following design rules to ensure clarity and correct processing.

5.1 DESIGN AREA

The standard user cell has dimensions of **11.47 x 15.45 mm².**

5.1.1 PHYSICAL DIE SIZE

The physical size of the dies you will receive is approximately 11.4 x 16.5 mm², as shown in Figure 1.

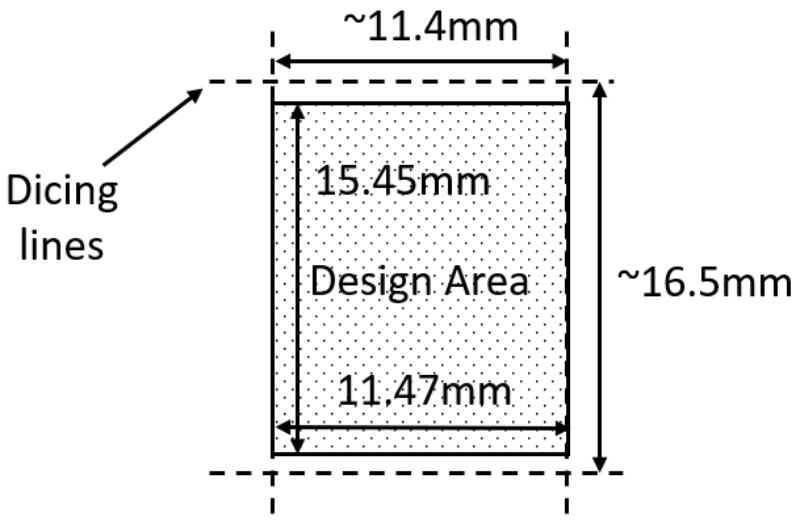


Figure 1– Dicing process and physical die dimensions after dicing.

The east and west facets will be diced to produce optical facets for edge coupling. Therefore, if you require edge couplers, ensure that your waveguides extend fully into the bleed region defined as a 35 µm strip at the edge of the east and west edges, as shown in Figure 2. As this region will be diced, ensure that no other devices extend into this region.

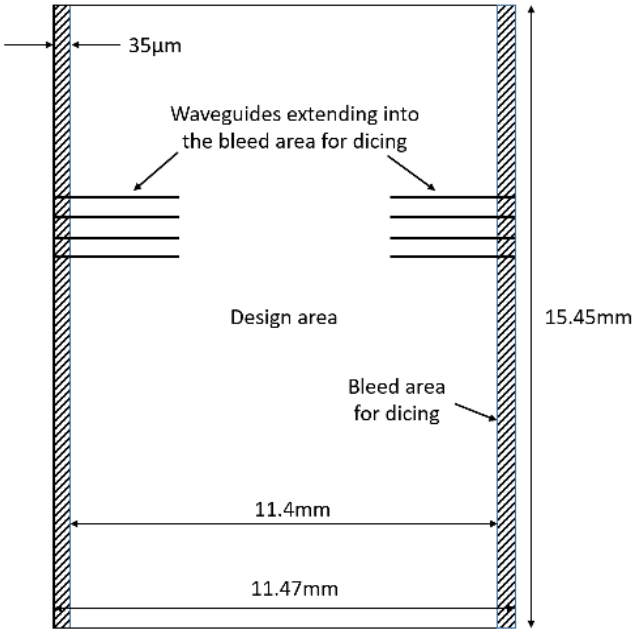


Figure 2 – Bleed area for the dicing process for edge couplers.

5.2 GDS LAYERS

Each lithographic step in the fabrication process flow is identified by a specific GDS layer/s. These are as follows:

Germanium Etch 1 (Waveguide layer) – GDS Layer 303 (Light field) & GDS Layer 304 (Dark field) – etch depth: 1.8 µm ± 200 nm.

This layer defines waveguides and is split into two separate GDS layer numbers, patterned into the same resist and etched together:

GDS Layer 303: Drawn objects on this layer will be protected from the germanium etch. Users should draw the waveguides and any other features to remain following 1.8 µm germanium etching. During fracturing processing, this will be translated into a pattern that defines 20 µm wide trenches on either side of the waveguides drawn in GDS layer 303 (see Figure 3).

If you require waveguide trenches that are a different width, refer to the guidelines for generating the trenches in Section 8. You can complete these steps yourself and modify the growth function dimension in step 1.

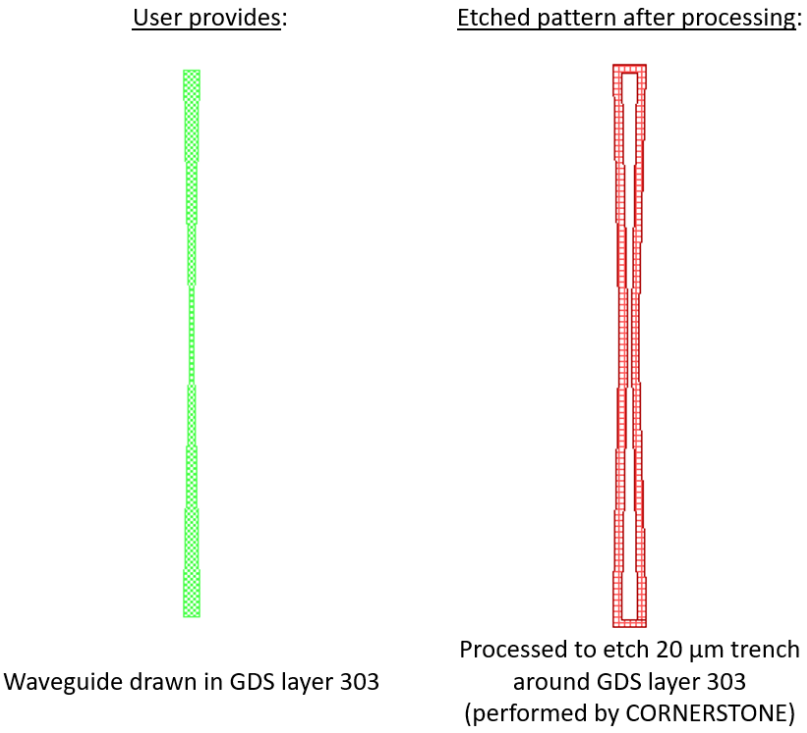


Figure 3 – Description of GDS Layer 303 processing.

GDS Layer 304: Drawn objects on this layer will be exposed to the 1.8 µm germanium etch. An example photonic crystal structure is shown in Figure 4. The important thing to note here is that the waveguide layer drawn in GDS layer 303 should overlap the structures drawn in GDS layer 304, so that when the 20 µm trenches are generated by CORNERSTONE, a continuous waveguide remains.

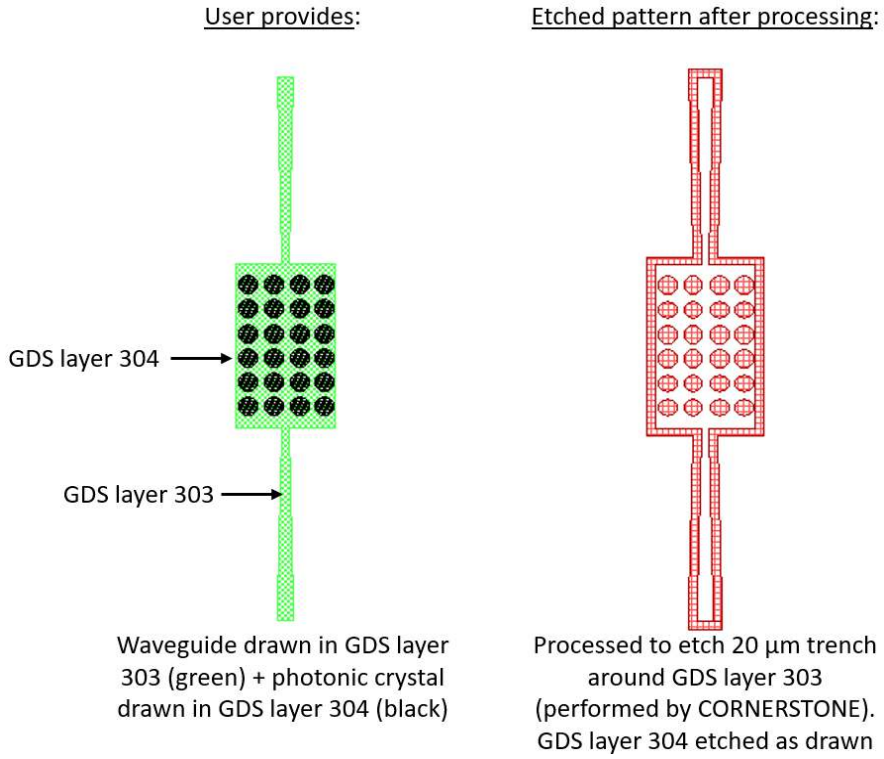


Figure 4 – Example photonic crystal structure using GDS Layers 303 & 304.

Bleed area – GDS Layer 98

This layer defines the bleed area that will be diced on the east and west facets, as shown in Figure 2.

Cell Outline – GDS Layer 99

This layer defines the design space boundaries (15.45 x 11.47 mm^2).

Labels – GDS Layer 100

This layer defines text labels, which will be merged with Germanium Etch 1 (Waveguides) by the CORNERSTONE team.

Note: You do not need to add fabrication alignment marks to your design. Layer-to-layer alignment marks will be added by the CORNERSTONE team, placed outside the design area.

5.3 MINIMUM FEATURE SIZES, TARGET CRITICAL DIMENSIONS AND OTHER DESIGN RULES

- Minimum feature sizes, minimum gaps, and maximum feature widths for each GDS layer are detailed in Table 2.
- The target critical dimension for each GDS layer is listed in Table 2. Note that other feature sizes may have a small dimensional bias.

5.4 DESIGN RULES SUMMARY

A summary of the design rules and GDS layer numbers described in this section is detailed in *Table 2* below.

Table 2 – Design rules summary.

Layer description	GDS number	Field	Min. feature size	Min. gap
Germanium Etch 1 (1.8 µm ± 200 nm)	303	Light	700 nm	700 nm
	304	Dark	700 nm	700 nm
Bleed area	98	N/a	N/a	N/a
Cell Outline	99	N/a	N/a	N/a
Labels*	100	Dark	700 nm	700 nm

*Features drawn in the Labels layer will be merged into Germanium Etch 1 by the CORNERSTONE team.

In order to help you ensure that you comply with the design rules, you can download and execute the KLayout pre-DRC script or use L-edit DRC file provided by CORNERSTONE on our website www.cornerstone.sotonfab.co.uk/design-rules (note that the automatic DRC will not check all of the design rules, so it remains very important to read the design rules in detail).

MPW users will have an opportunity to attend 1-to-1 Drop-in Sessions to pre-review mask layouts before the submission deadline, using this link to book a 20-mins session.

5.5 FILE FORMAT

Designs must be submitted in a Graphical Database System file (extension *.gdsII*) or Open Artwork System Interchange Standard (extension *.oas*) format. Ensure a manufacturing grid size of 1 nm is used, as per the CORNERSTONE GDSII Template file.

We recommend dedicated lithography editing software be used in the design of the *.gdsII* or *.oas* file.

5.6 GDSII TEMPLATE FILE

A *.gdsII* template file has been made available on our website containing the information described in this section. Ensure that all submitted designs fit within the specified area, and that only the designated GDS layer numbers are used.

6 QUALITY ASSESSMENT

This fabrication run will be qualified by characterising a standard test pattern that is included on the chip (not part of the user cell). The test structures that will be checked after fabrication are reported in Table 3 below, together with the values that are targeted by the CORNERSTONE platform.

Table 3 – Quality assessment parameters.

Test structure	Parameter	Value
Straight single mode rib waveguide	Propagation loss	< 5 dB/cm for TE mode at λ = 3.8 μm

7 MASK SUBMISSION PROCEDURE

In order to be eligible to submit a design you must first sign-up to this call using the online form found using the link below. This is in order to enable us to prepare the necessary paperwork and plan the fabrication process effectively. The sign-up deadline is found at the top of this document.

www.cornerstone.sotonfab.co.uk/mpw-sign-up-form

Under no circumstances will we accept any design submissions for which we have not received a sign-up form.

After completing the sign-up form, when you are ready to submit your mask design on or before the mask submission deadline listed at the top of this document, follow the link below to the CORNERSTONE website mask submission page:

www.cornerstone.sotonfab.co.uk/gds-file-upload

A purchase order (PO) must be uploaded to this form to pay the access fee. Purchase orders will not be accepted via email.

You must also upload your design file to the submission form. Ensure that the top cell in your design file is titled 'Cell0_*[Name of Institution]*'.

For information about setting up CORNERSTONE as a supplier to your institution, please contact cornerstone@soton.ac.uk.

8 MASK PROCESSING PERFORMED BY CORNERSTONE

Upon receipt of your *.gdsII* file, the CORNERSTONE team will perform the following mask processing steps in order to produce the final mask, based on the descriptions provided in Section 5.2:

Germanium Etch 1 (Waveguide layer) – GDS Layer 303 (Light field) & GDS Layer 304 (Dark field) – etch depth: 1.8 µm ± 200 nm:

1. Grow Waveguide Etch layer (GDS layer 303) by 20 µm in all directions.
2. Subtract the Waveguide Etch layer (GDS layer 303) from the output of (1) to produce the etch trenches around the drawn waveguides.
3. Merge the output of (2) with the dark field Waveguide Etch layer (GDS layer 304) and the Labels layer (GDS layer 100).

9 TECHNICAL SUPPORT

If you have any questions relating to the fabrication process or design rules, please contact the CORNERSTONE team (cornerstone@soton.ac.uk).

10 CHIP DELIVERY

A total of 5 replica cells will be delivered to each user. The delivery time schedule can be found in Table 1.

11 FEEDBACK

Feedback is essential to the CORNERSTONE team. It is required to ensure a continuous improvement to the quality of our services. It is also evidence on the user satisfaction, and a measure to what extent we were able to meet user requirements. Therefore, we kindly ask our users to provide feedback to us, including device performance data, SEM images, future interests for the CORNERSTONE project etc. A feedback form will be sent to you along with your chips.

Alternatively, email cornerstone@soton.ac.uk with your comments.

12 PUBLICATIONS

If you are benefitting from subsidised access via the C-PIC funding, please include the following statement in the "Funding" section of any publications:

"The chip fabrication for this research was funded by the Engineering and Physical Sciences Research Council (EPSRC) C-PIC (EP/Z531066/1) project."

This is important to us to be able to demonstrate impact from the funding.

If you are a paying user, we kindly ask that you include CORNERSTONE in the "Acknowledgments" section of any publications that result from the chips you receive from CORNERSTONE.